Claims

We claim:

1. A method for forming an electronic device, comprising:

providing a layer of gate dielectric;

forming a layer of amorphous silicon on the layer of gate dielectric;

forming a gate cap dielectric on the layer of amorphous silicon;

providing at least one spacer adjacent the layer of amorphous silicon; and

exposing the amorphous silicon to a temperature sufficiently high to convert the amorphous silicon to polysilicon after the at least one spacer has been provided.

2. The method of claim 1, wherein the exposing step comprises exposing the amorphous silicon to a temperature of at least approximately 750° C to convert the amorphous silicon to polysilicon after the at least one spacer has been provided.

3. The method of claim 1, wherein the exposing step comprises exposing the amorphous silicon to a temperature of at least approximately 800° C to convert the amorphous silicon to polysilicon after the at least one spacer has been provided.

4. The method of claim 1, wherein the exposing step comprises performing a rapid thermal anneal at a temperature sufficiently high to convert the amorphous silicon to polysilicon after the at least one spacer has been provided.

5. The method of claim 1, further comprising performing a gate sidewall oxidation at a temperature sufficiently low to avoid transformation of the amorphous silicon to polysilicon before providing the at least one spacer.

6. The method of claim 1, wherein the at least one spacer is provided at a temperature of less than approximately 750° C.

7. The method of claim 1, further comprising:

performing lithography and etching after the gate cap dielectric has been formed; and

implanting a source and a drain into the electronic device after the at least one spacer has been provided.

8. The method of claim 1, wherein the gate cap dielectric is selected from the group consisting of silicon nitride and silicon dioxide.

9. The method of claim 1, wherein the electronic device is a field-effect transistor (FET) device.

10. A method for forming an electronic device, comprising:

providing a layer of gate dielectric;

forming a layer of amorphous silicon on the layer of gate dielectric;

forming a gate cap dielectric on the layer of amorphous silicon;

providing at least one spacer adjacent the layer of amorphous silicon; and

performing a rapid thermal anneal at a temperature of at least approximately 750° C after the at least one spacer has been provided to convert the amorphous silicon to polysilicon.

11. The method of claim 10, wherein the exposing step comprises performing a rapid thermal anneal at a temperature of at least approximately 750° C to convert the amorphous silicon to polysilicon after the at least one spacer has been provided.

12. The method of claim 10, further comprising performing a gate sidewall oxidation at a temperature below approximately 750° C to avoid transformation of the amorphous silicon to polysilicon before providing the at least one spacer.

13. The method of claim 10, further comprising:

performing lithography and etching after the gate cap dielectric has been formed and

implanting a source and a drain into the electronic device after the at least one spacer has been provided.

14. The method of claim 10, wherein the gate cap dielectric is selected from the group consisting of silicon nitride and silicon dioxide.

15. The method of claim 10, wherein the electronic device is a field-effect transistor (FET) device.

16. A method for forming a field-effect transistor (FET) device, comprising:

providing a layer of gate dielectric;

forming a layer of amorphous silicon on the layer of gate dielectric;

forming a gate cap dielectric on the layer of amorphous silicon;

providing a first spacer adjacent the layer of amorphous silicon;

providing a second spacer adjacent the layer of amorphous silicon; and

exposing the amorphous silicon to a temperature of at least approximately 750° C after the second spacer has been provided to convert the amorphous silicon to polysilicon.

17. The method of claim 16, wherein the exposing step comprises performing a rapid thermal anneal at a temperature of at least approximately 750° C to convert the amorphous silicon to polysilicon after the at least one spacer has been provided.

18. The method of claim 16, further comprising performing a gate sidewall oxidation at a temperature below approximately 750° C to avoid transformation of the amorphous silicon to polysilicon before providing the at least one spacer.

19. The method of claim 16, further comprising:

performing lithography and etching after the gate cap dielectric has been formed;

implanting an extension into the FET device after the first spacer has been provided; and

implanting a source and a drain into the FET device after the second spacer has been provided.

20. The method of claim 16, wherein the gate cap dielectric is selected from the group consisting of silicon nitride and silicon dioxide.